Code No : 20EE6P01 **R20**

III B. TECH II SEMESTER REGULAR EXAMINATIONS APRIL - 2023
DIGITAL ELECTRONICS
(ELECTRICAL AND ELECTRONICS ENGINEERING)

Time: 3 hours Max. Marks: 70

Note: Answer **ONE** question from each unit **(5 × 14 = 70 Marks)**

UNIT-I

1. a) i) Convert $(F57)_{16}$ into decimal. [7M]
   ii) Convert $(6348)_{10}$ into Octal.

   b) Obtain the 9's and 10's complement of $(389.61)_{10}$. [7M]

(OR)

2. a) i) List the truth table of F = (xy + xy' + y'z)' [7M]
   ii) Draw logic diagrams to implement the Boolean expression Y = A + B + B'(A +C')

   b) Implement the given function using NOR gates only. [7M]
   F(X, Y, Z) =Σm(0,3,6).

UNIT-II

3. a) Obtain the simplified expression in product of sums. [7M]
   F(A,B,C,D) = π(0,2,5,6,9,12,13)

   b) Obtain the simplified expression in sum of products for the following Boolean function. [7M]
   BDE+B′ C′ D+CDE+A′ B′ CE+A′ B′ C+B′ C′ D′ E′

(OR)

4. a) Using K-map method, Reduce the following Boolean function. [7M]
   F=∑m(0,2,3,6,7) + d(8,10,11,15) and obtain minimal SOP

   b) Explain a four-bit binary adder circuit with relevant diagram. [7M]

UNIT-III

5. a) Design the logic circuit for full subtractor using truth table. [7M]

   b) Implement a 2-bit magnitude comparator [7M]

(OR)

6. a) Design16 x 4 encoders using two 8 x 3 encoders. [7M]

   b) Implement Boolean function F(A,B,C,D)=Σm(0,1,3,4,8,9,15) using 8:1 multiplexer. [7M]

UNIT-IV

7. a) Design MOD-10 asynchronous counter using JK flipflop. [7M]

   b) Explain in detail the operation of a 4-bit binary ring counter. [7M]

(OR)

8. a) Design a D flip flop using JK flip flop and explain with its truth table [7M]

   b) What is shift register? Explain the working of 4-bit bidirectional shift register. [7M]

UNIT-V

9. a) Explain state diagram, state table and state assignment with example. [7M]

   b) Write difference between Mealy and Moore machines in detail. [7M]

(OR)

10. a) Design an FSM for serial sequence detector with the pattern “0110” with non-overlapping. use Mealy Machine. [7M]

    b) Write design procedure of a finite state machine. [7M]

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